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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,390	10/31/2003	Yung-Hung Chen	250606-1010	3274
24504	7590	11/10/2004	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			TRA, ANH QUAN	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/699,390

Applicant(s)

CHEN, YUNG-HUNG

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 is indefinite because there is no antecedent basis for the limitation “the differential amplifier”.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuchi (USP 6614295).

As to claim 1, Tsuchi discloses in figure 10 a voltage reference generator for generating an output voltage (Vout) at an output node, comprising: a level shifter (42 and 32) for shifting a first reference voltage (voltage at the gate of 421) into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and a feedback

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circuit (22) for monitoring the output voltage and a second reference voltage ( $V_{in}$ ) to control the shift and to normalize the output and second reference voltages.

As to claim 2, figure 10 shows that the level shifter includes a source follower (422) coupled between a voltage source (VDD) and the output node, the source follower having an input node (gate) for receiving the first reference voltage.

As to claim 3, figure 10 shows that the source follower has an MOS transistor having a drain connected to the voltage source, a source as the output node and a gate at the input node, and further having a current source (321) controlled by the feedback circuit and connected to the source of the MOS transistor.

As to claim 4, figure 10 shows the MOS transistor is a NMOS transistor.

As to claim 5, figure 11 shows a similar voltage reference generator with the source follower (412) is a PMOS transistor.

As to claim 6, figure 10 shows that the current source (321) is an MOS transistor having a drain connected to the output node, a source connected to a ground, and a gate connected to the output of the differential amplifier.

As to claim 7, figure 11 shows a similar voltage reference generator with a level shifter (41) further comprising a constant current source (415) coupled between the output node and another voltage source.

As to claim 8, figure 10 shows that the MOS transistor is a NMOS transistor.

As to claim 9, figure 11 shows a similar voltage reference generator having an PMOS current source (311).

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As to claim 12, figure 10 shows that the feedback circuit has a differential amplifier (22) with an inverted input, a non-inverted input and an output, the non-inverted input coupled to the output node, the inverted input coupled to the second reference voltage, and the output coupled to a current source (32) in the level shifter to control the shift of the level.

As to claim 14, figure 10 shows a voltage divider (424, 421, 423) to provide the first reference voltage and a third reference voltage (voltage at the source of 421).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi (USP 6614295) in view of Forbes (USP 6362691).

As to claim 10, Tsuchi's figure 10 shows all limitations of the claim except for a low-pass filter to filter out a high frequency portion of the first reference voltage and direct the first reference voltage to the level shifter. However, Forbes's figure 2 shows a filter circuit (28) coupled to the gate of a voltage follower to filter its gate voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a filter circuit for Tsuchi's voltage follower for the purpose of filtering its gate voltage.

As to claim 11, the modified Tsuchi's figure 10 shows that the low-pass filter comprises at least a capacitor connecting an input node of the level shifter and a voltage source.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi (USP 6614295) in view of Khalid (US 2004/0150464).

Tsuchi's figure 10 shows all limitations of the claim except for a low-pass filter connected between output of the differential amplifier and current source in the level shifter. However, Khalid's figure 1B shows a low-pass filter 12 coupled to the output of differential amplifier 11 and to the gate of current source 13 in order to filter the output voltage of the amplifier 11. Therefore, it would have been obvious to one having ordinary skill in the art to add a low-pass filter to the output of Tsuchi's differential amplifier for the purpose of filtering the output of the amplifier.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', with a long horizontal flourish extending to the right.

Quan Tra  
Patent Examiner

November 5, 2004